Field Engineering

Maintenance Diagrams

Computing System
Features

## PREFACE

Synchronous Communications Adapter IBM 2501 Card Reader Adapter IBM 1231 Optical Mark Page Reader Adapter

Use the system diagrams at the engineering level of the equipment being serviced when there is a difference between the system diagrams and the maintenance diagrams in this manual.

## Fourth Edition (May 1970)

This manual is a complete revision of SY26-4003-2 and obsoletes the previous edition.

Specifications contained herein are subject to change from time to time. Any such change will be reported in subsequent revisions or Field Engineering Supplements.

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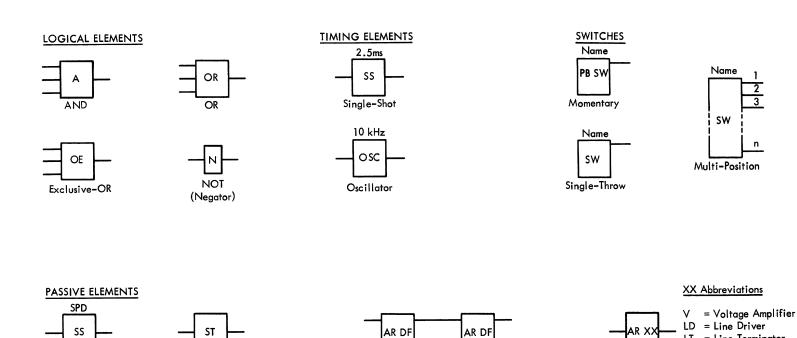
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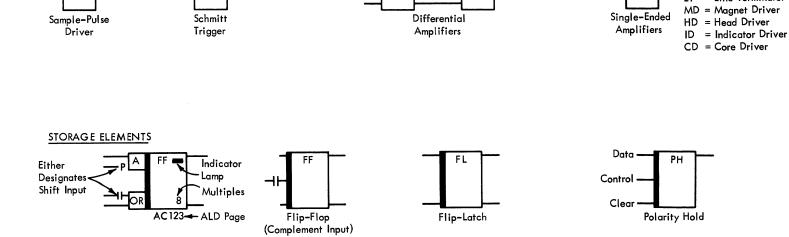
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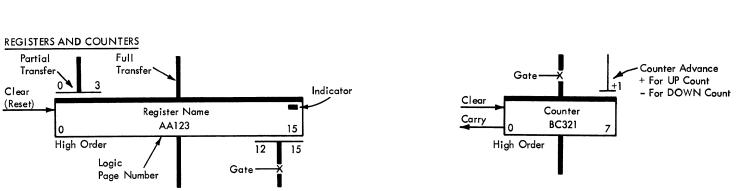
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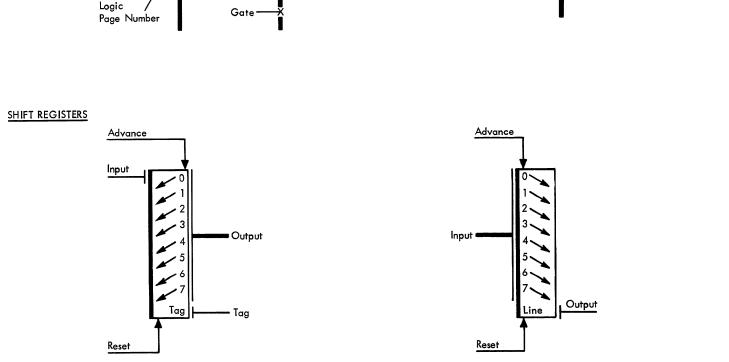
In positive logic representation, signal levels are disregarded. The negator (N block symbol) is used to invert logic, not level. Passive elements (such as drivers and pulse shapers) generally are not shown, since they contribute nothing to the logic.

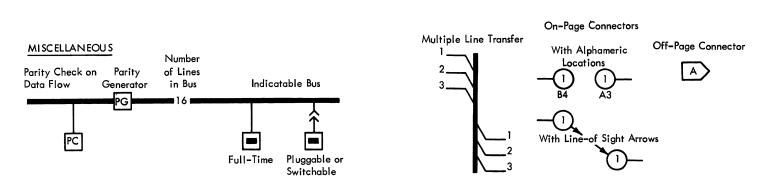


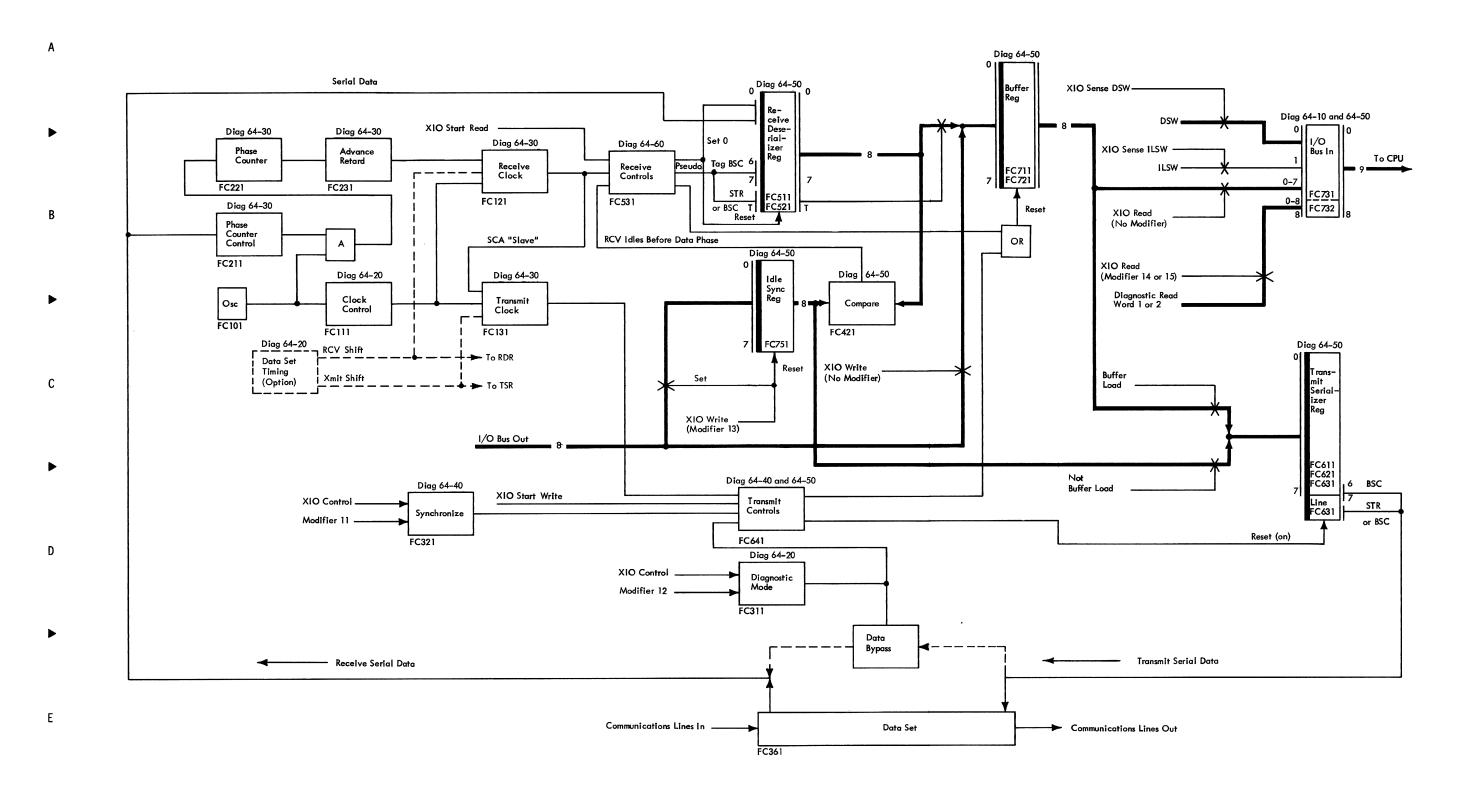
LT = Line Terminator

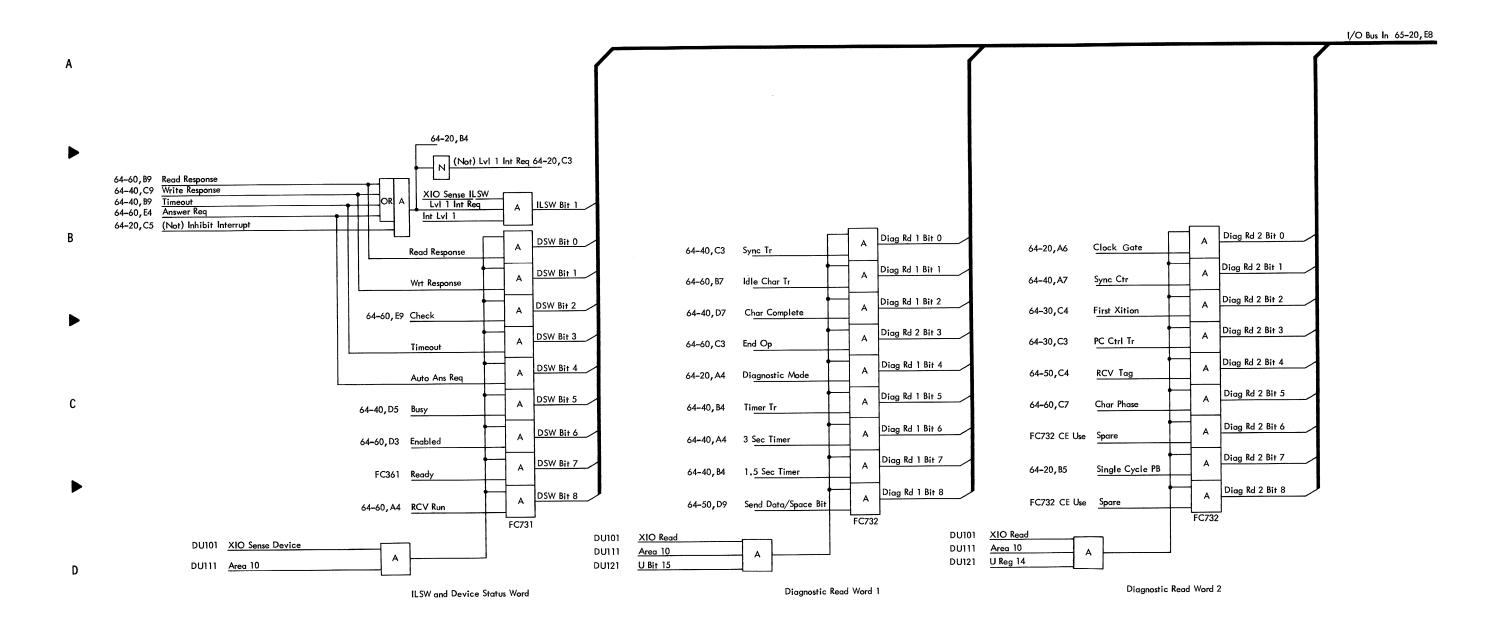




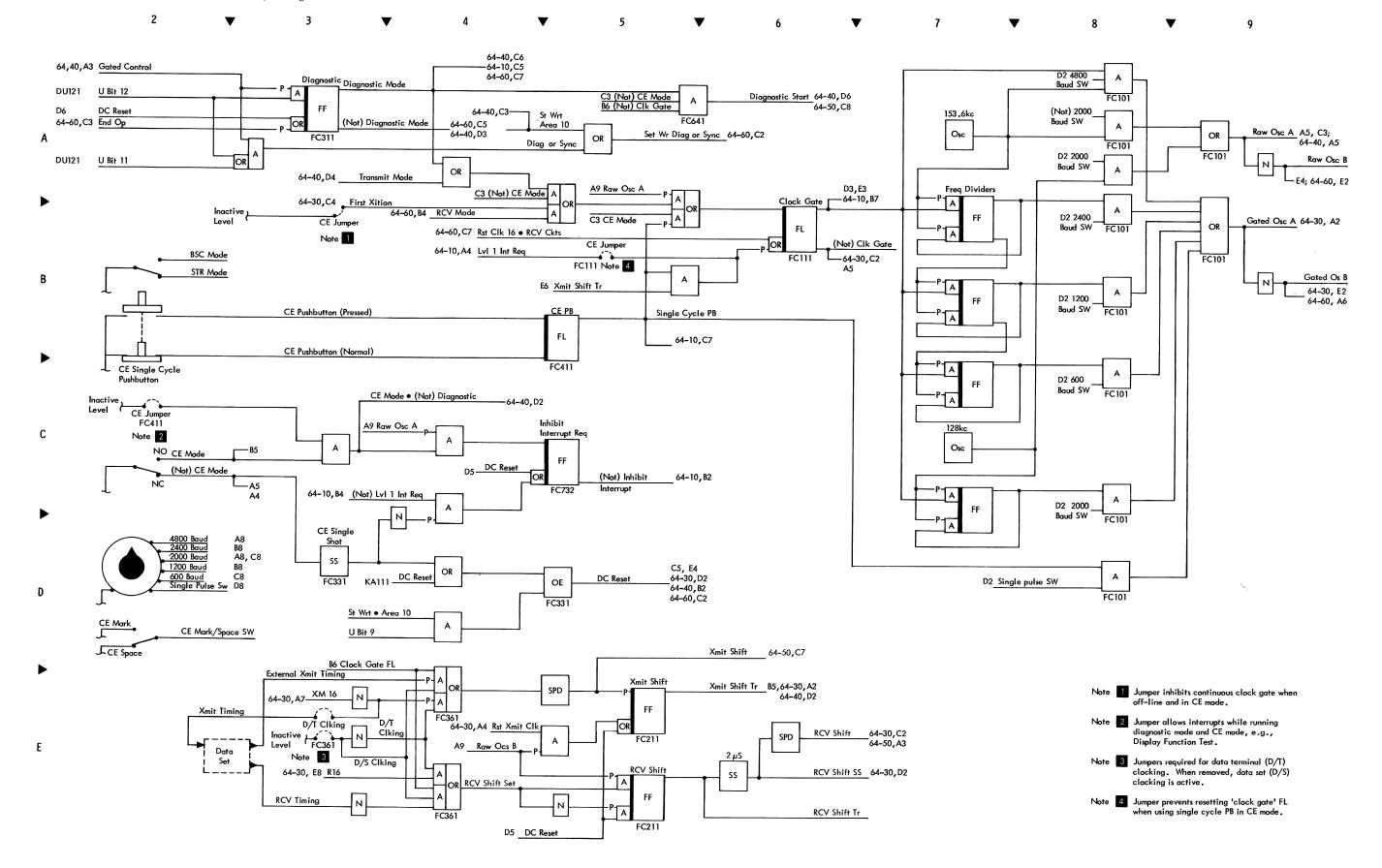




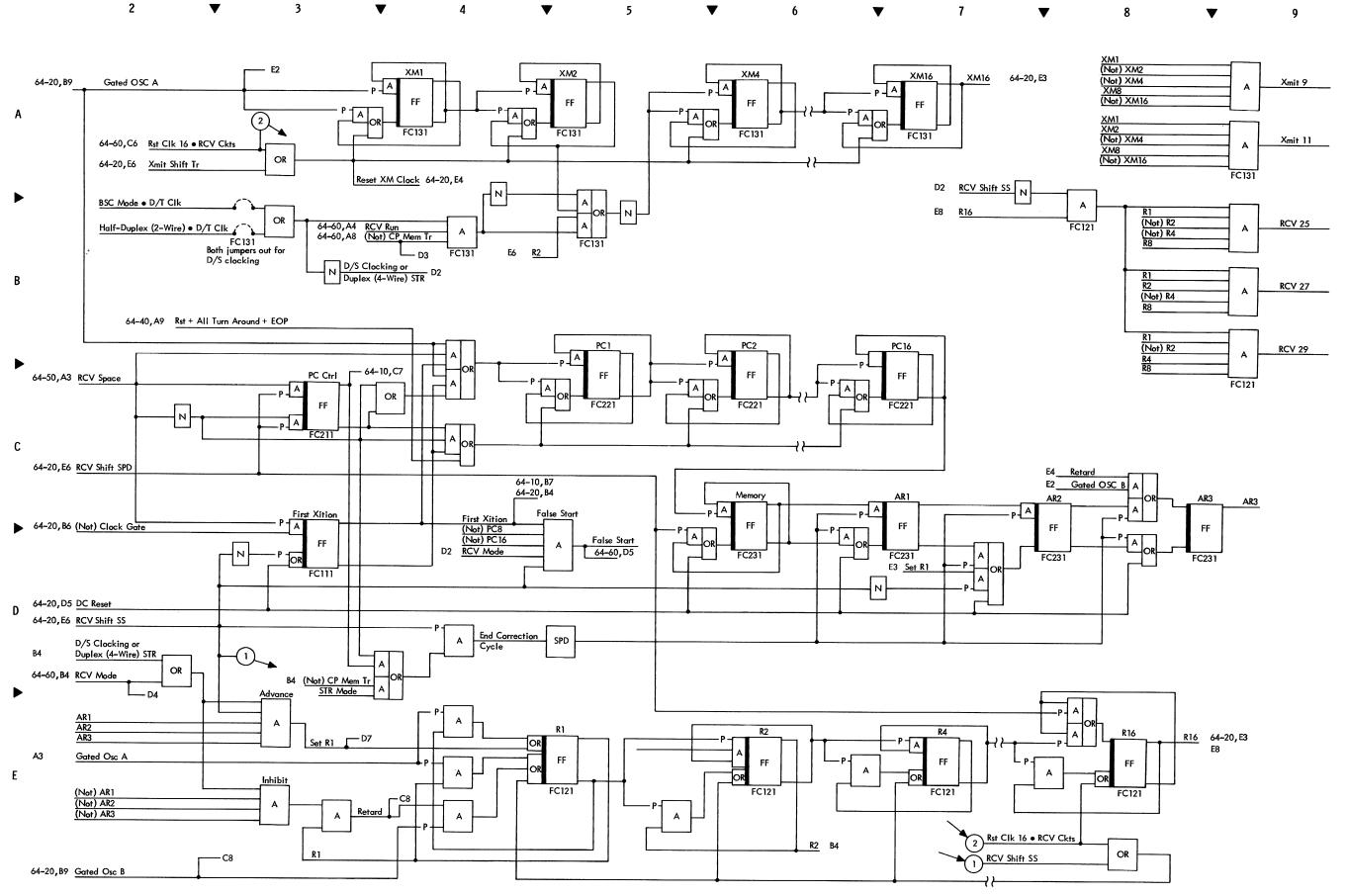


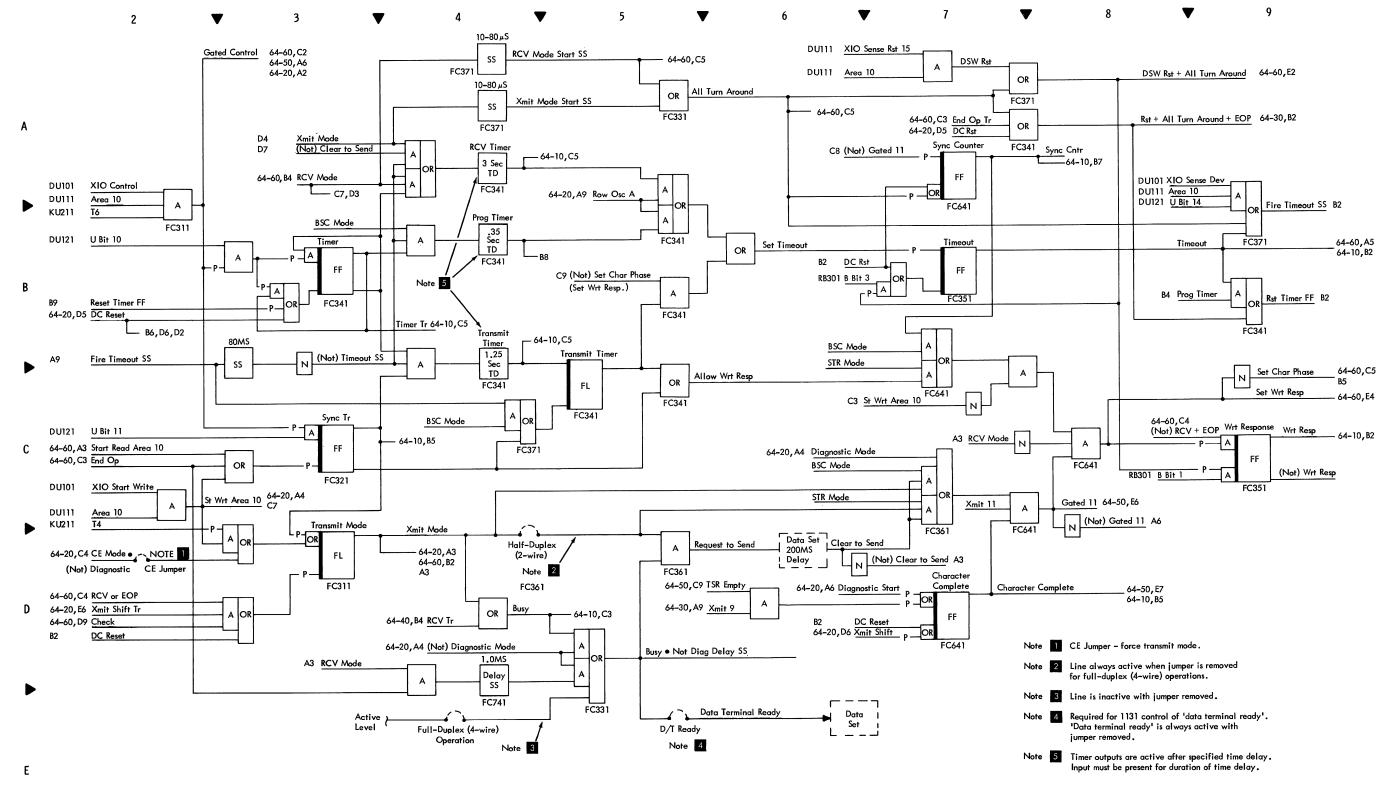


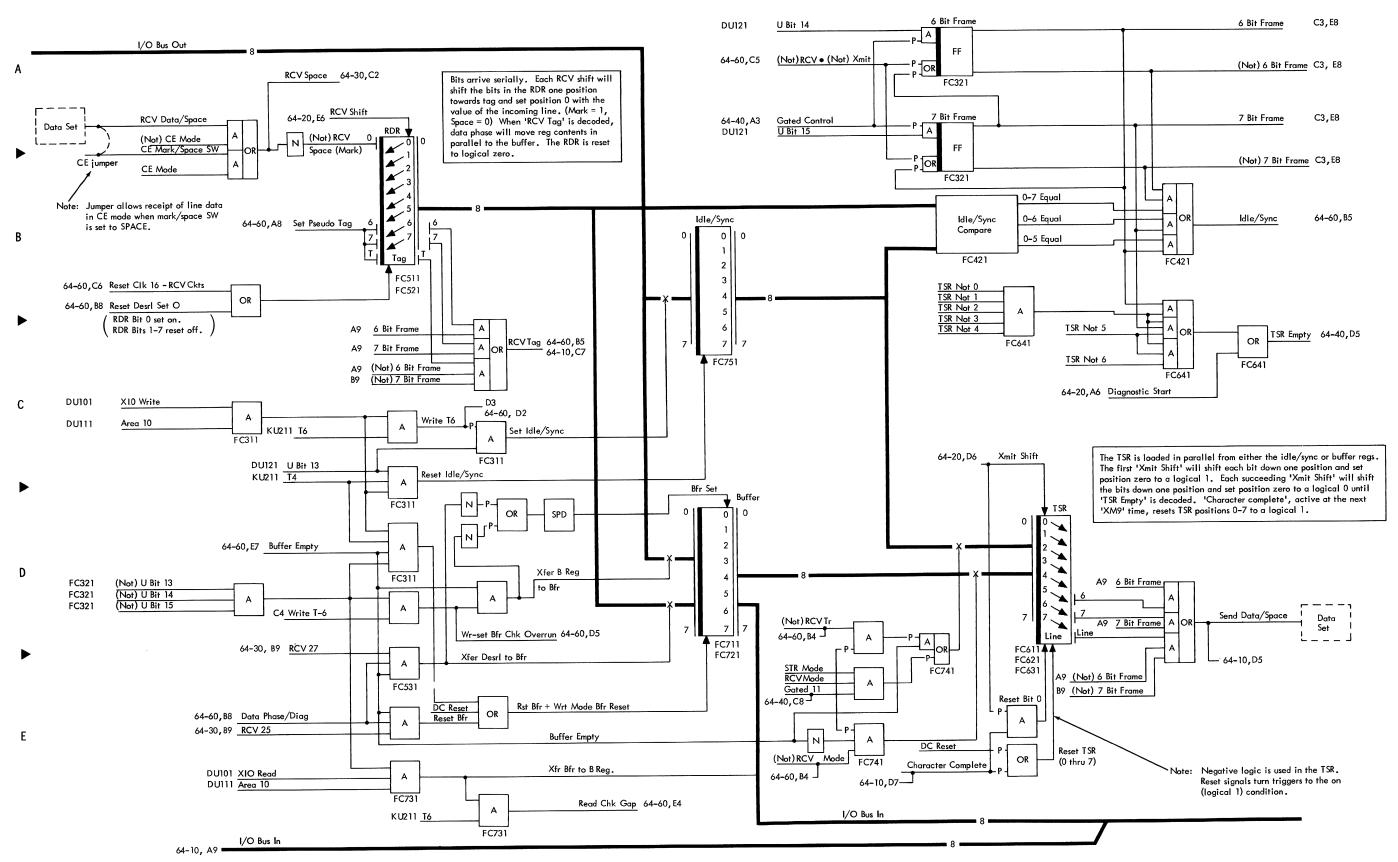
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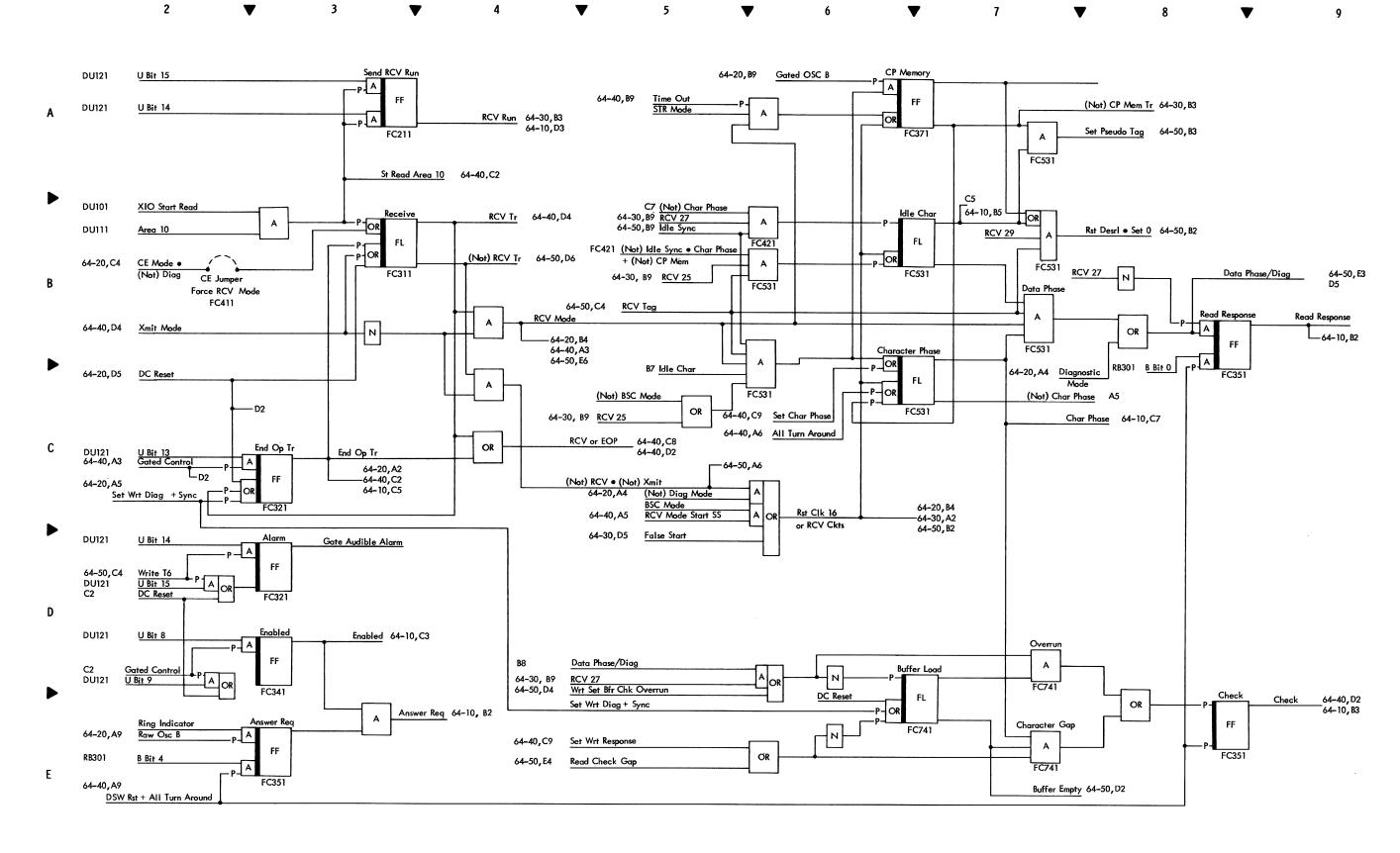












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- 1. Transmit contents of idle-sync register repeatedly.
- 2. Block write responses for 1.25 sec.
- When write responses are allowed, continue transmitting characters from CPU core storage under program control.

#### 'Synchronize' Operation - STR (64-40)

- Turn on 'synchronize trigger' FF (C3) and 'transmit' FL (D3) and reset off the 'buffer load' FL (64–60, D7).
  - 2. Start 1.25 sec timer (B4) and fire transmit mode start SS (A4).
- 3. Start clocks, if not already started (64-20, A4).
- Activate 'request to send' line (D5) if not already active. In full duplex (4-wire), this occurs when the SCA first becomes busy and is not in diagnostic mode.
- After about 200 ms, data set activates 'clear to send', if not already active. 'Clear to send' remains active as long as 'request to send' remains active.
- 6. With TSR empty, at 'Xmit 9', turn on 'character complete' (D6).
- 7. At 'gated 11', attempt to set 'write response' but cannot (C8).
- With buffer empty, at 'gated 11', transfer sync register to TSR (64–50, E6).
- 9. Repeat steps 6, 7, and 8 until 1.25 sec timer times out.
- Turn on 'transmit timer' latch (C5). Allow write responses until turned off.
- 11. At the end of the 'gated 11' which sets write response the first time, turn on 'character phase' FF (64-60, C6).
- With the next 'start read write end op', turn off 'synchronize trigger' FF. This turns off the 'Xmit timer latch'.

#### 'Start Write' Objectives - STR

- 1. Transmit contents of idle-sync register once.
- Start transmitting characters from CPU core storage under program control.

#### 'Start Write' Operation - STR (64-40)

- Turn on 'transmit' FL (D3), activating transmit mode. Reset 'buffer load' FL off (64–60, D7).
- 2. Fire transmit mode start SS (A4), activating 'all turn around'.
- Reset controls for other operation, such as 'receive' or 'end op' (64–60, B2, C2). Turn off 'char phase' FL, but not 'CP Mem' FF (64–60, C6).
- In half duplex (2-wire) system, activate 'request to send' (D5).
   In full duplex (4-wire) system, 'request to send' is always active.
- Approximately 200 ms after 'request to send' is activated, data set activates 'clear to send', which remains active as long as 'request to send', is active.
- 6. With TSR empty, at 'Xmit 9', turn on 'character complete' (D6).
- At 'gated 11', set write response (C9), which causes interrupt level 1 (64–10, B3). (Character gap check is inhibited because 'character phase' is off.)
- With buffer empty, at 'gated 11', transfer sync reg to TSR (64–50, E6). At end of first 'gated 11', turn on 'character phase' (64–60, C6).
- While the one idle-sync character is being transmitted, program must load buffer register with next character from CPU core storage, to prevent 'character gap'.
- At each 'character complete' set 'write response' and interrupt. Check for 'character gap' (64–60, E7).
- While each character is being transmitted, program must load buffer register with next character.
- 12. Should 'character gap' occur, load TSR from the idle-sync register.
- 13. When the program recognizes that the last character has been transferred to the buffer register, a 'start read' instruction is usually given.
- 14. With 'receive' FL on, block 'Xfer sync reg to Xmit ser'
  until 'RCV mode' becomes active (64-60, B4). (In 4-wire STR,
  these transfers are necessary during receive mode.)
- 15. 'Character gap' check is set at 'set write response' time when the last bit of the last character is in the line position of the TSR, 'TSR empty' (64–50, C9).
- 'Xmit shift tr' becoming active again turns off the 'transmit' FL (D3) and activates 'receive mode' (64-60, B4).

#### 'Synchronize' Objectives - BSC

- 1. Transmit contents of idle-sync register at least twice.
- 2. Block one write response.
- When write responses are allowed, continue transmitting characters from CPU core storage under program control.
- 4. If still transmitting after 1.25 sec, cause timeout interrupt.

#### 'Synchronize' Operation - BSC (64-40)

- 1-8. Same as 'Synchronize' Operation STR.
- At end of first 'gated 11', turn on 'sync counter' FF (A7). This 'gated 11' cannot 'set write response' because 'sync counter' is off.
- 10. At each following 'gated 11' set 'write response' (C9).
- 11. At the end of the 'gated 11' which sets write response the first time, turn on 'character phase' FF (64-60, C6).
- 12. Continue transmitting as in steps 10–16 of 'start write' operation STR.
- With next 'start read write end op', turn off 'synchronize trigger'
   FF (C3)
- 14. If the next instruction does not occur before 1.25 sec have elapsed, turn on 'Xmit timer latch' and set 'timeout' FF (B7) when the next 'set write response' occurs, causing an interrupt.
- 15. The program can use the interrupt to insert 'sync' characters in the transmitted data.
- The program can cause a timeout interrupt after 0.35 sec by an instruction which turns on the program timer (B4).

### 'Start Write' Objectives - BSC

- 1. Transmit contents of idle-sync register twice.
- Start transmitting characters from CPU core storage under program control.

#### 'Start Write' Operation - BSC (64-40)

- 1-6. Same as 'Start Write' Operation STR.
- At first 'gated 11', prevent setting 'write response' (C9). With buffer empty, transfer idle-sync register to TSR (64-50, D7).
- 8. At end of first 'gated 11', turn on 'sync counter' FF (A7).
- At second 'gated 11', set 'write response', which causes interrupt level 1 (64-10, B3).
- At second 'gated 11' again transfer idle-sync reg to TSR. At end of this 'gated 11', turn on 'character phase' FF (64-60, C6).
- While second idle-sync character is being transmitted, program must load buffer with next character from CPU core storage.
- 12. Continue as in steps 10–16 of 'Start Write' Operation STR. However, in step 14, the 'Xfer sync reg to Xmit ser' line is not reactivated in receive mode (64–50, E6).

## 'Write' Objectives - STR or BSC

- 1. Check for overrun.
- 2. Load buffer register with next character from CPU core storage.

#### 'Write' Operation - STR or BSC (64-50)

- At T4 of CPU E-3 cycle, if 'buffer load' FL is off (64-60, E7), reset buffer register (D5). ('Buffer load' off indicates previous character has read out, and 'buffer empty' is active.
- 2. At T6, if 'buffer load' FL is on, turn on 'check' FF (Overrun).
- At T6, if 'buffer load' FL is off, gate 'transfer B register to buffer' (D5).
- 4. At end of T6, if 'buffer load' FL is off, activate 'buffer set'
  SPD (D4) and turn on 'buffer load' FL (64-60, E6).

#### 'Write-Modifier 13' Objective - STR or BSC

Load idle-sync register with a character from CPU core storage.

#### 'Write-Modifier 13' Operation - STR or BSC (64-50)

- At T4 of CPU E-3 cycle, with 'U bit 13' active, reset idle-sync register (C4).
- At T6, with 'U bit 13' active, set idle-sync register from B register outputs (C4).

2

#### 'Start Read' Operation - STR (64-60)

- Turn on 'receive' FL (B3). If 'transmit' FL is off, activate 'receive mode' immediately. If 'transmit' is on, wait to activate 'receive mode' when 'transmit' turns off.
- 2. Fire receive mode start SS (64-40, A4). Activate 'all turn around'.
- Reset controls for other operations. Turn off 'character phase' FL, but not 'CP memory' FF, if they are on (C6 and A6).
- Start receiving and shifting bits through RDR, comparing RDR with idle-sync register (64-50, B3, B7).
- If 'CP memory' FF is off (not previously in 'character phase', or else a timeout occurred during the last 'receive mode'):
  - A. With equal idle-sync compare, turn on 'idle character' FL at RCV 27 (86).
  - B. With 'idle character' on activate 'set pseudo tag' (A7).
  - C. Turn on 'character phase' and 'CP memory' (C6 and A6).
- If 'CP memory' FF is on (previously in 'character phase' and no timeout occurred during the last 'receive mode'):
  - A. With equal idle-sync compare, turn on 'idle character' FL at RCV 27 (B6).
  - B. Framing was previously completed (tags shifting through RDR).
  - C. With equal idle-sync compare and 'idle character' on, turn on 'character phase' and 'CP memory' at 'tag' time (A7 and C7).
- On receipt of the first non-idle character, at 'tag' time turn off 'idle character' at RCV 25 (B5).
- 8. Activate 'data phase' at RCV tag time (B7).
- 9. With 'buffer load' off and RCV 25, reset buffer register (64-50, E3).
- At RCV 27, if 'buffer load' is on, set overrun (D8). If 'buffer load' off, transfer RDR to buffer register (64-50, E4).
- At end of RCV 27, turn on 'buffer load' FL (D8) and 'read response'
   FF (B8), activating 'level 1 interrupt request'.
- Continue receiving until 'transmit' or 'end op' instruction turns off 'receive' FL (83).
- 13. 'End op' fires the 1,0 ms delay SS to maintain 'busy' for the duration of the SS (64–40, E4).

#### 'Start Read' Objectives - BSC

- Recognize two successive idle-sync characters to establish 'character phase'.
- 2. Starting with first non-idle character, receive following characters and set them in buffer register.

#### 'Start Read' Operation - BSC (64-60)

- Turn on 'receive' FL (B3). If 'transmit' FL is off, activate 'receive mode' immediately. If 'transmit' is on, wait to activate 'receive mode' when 'transmit' turns off.
- 2. Fire receive mode start SS (64-40, A4). Activate 'all turn around' and 'reset clock 16 and RCV circuits' (C5) stopping clocks.
- Reset controls for other operations. Turn off 'CP memory' FF and 'character phase' FL (A6 and C6).
- 4. On first mark to space transition, turn on 'clock gate' FL (64-20, B4) restart clocks. Use first transition circuits to ensure no false start from noise. (64-30, D4).
- Start receiving and shifting bits through RDR, comparing RDR with idle-sync register. When idle-sync compare is equal turn on 'idle character' FL at RCV 27 (B6).
- 6. Activate 'set pseudo tag' (A7). Framing is complete.
- If idle-sync compare is equal at the <u>next</u> RCV tag, turn on 'character phase' and 'CP memory' at RCV 25 (C6 and A6).
- If idle-sync compare is not equal at the <u>next</u> RCV tag turn off 'idle character' FL at RCV 25 (B5). Do not turn on 'character phase' and 'CP memory'.
- Continue comparison until idle-sync compare is equal when 'idle character' FL is on. Then turn on 'character phase' and 'CP memory'
- 10. Continue receive operation as in steps 7-13 of STR.

## 'Read' Objectives - STR or BSC

- 1. Check for character gap.
- Transfer a received character from the buffer register to CPU core storage.

9

## 'Read' Operation - STR or BSC (64-60)

- 1. During CPU E-3 cycle, transfer buffer to B register (64-50, E5).
- 2. At T6, if the 'buffer load' FL is off during 'character phase', activate 'character gap' and turn on 'check' FF (E7).
- 3. At the end of T6, turn off 'buffer load' FL (E6).

XIO Control End Op (Bit 13) XIO Start Read Α FC321 FC311 FC321 Tum off sync trigger FF. Turn on end op FF. Tum on receive FL. FC351 FC321 FC321 FC311 В Turn off end op FF. Inhibit write response FF. Turn off sync trigger FF. Turn off receive FL. Yes Yes Νo Transmit FL on? Transmit FL on? С Wait for char-racter gap. FC741 Wait for xmit shift (XM0). D FC311 Turn off transmit FL. End Op Receive or end op ? Ε Receive 4 Wire 2 Wire FC361 FC361 FC111 Request to send remains active. Drop request to send. Turn off clock gate. F FC361 Data set drops clear to send. Drop request to send. Stop clocks and reset to 0. BSC STR/BSC STR Continue send-ing mark char-acters on one pair of wires. Continue sending idle characters on one pair of wires. (End operation.) Data set drops clear to send. G FC311 Enter receive mode. Н 65-40, A4

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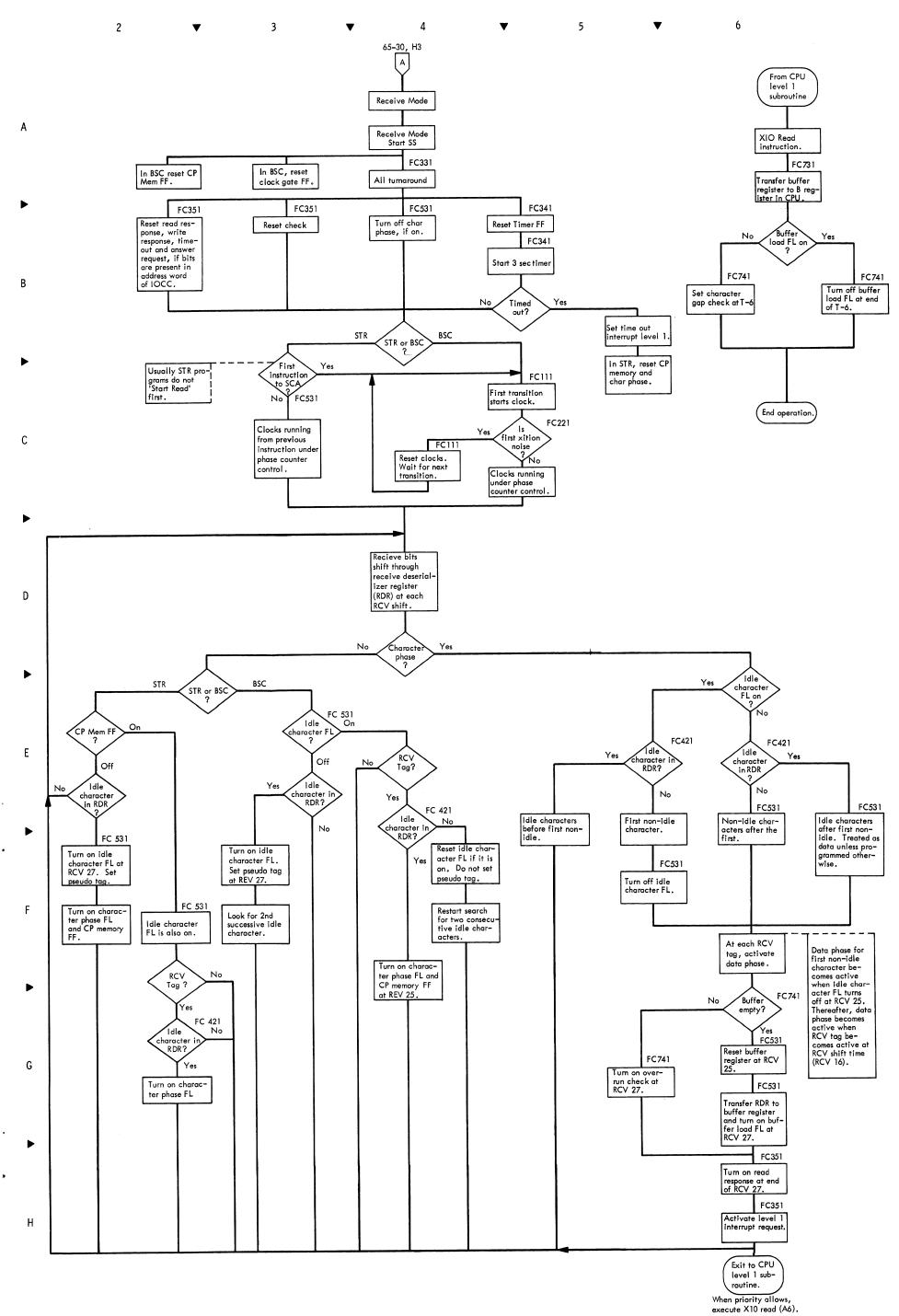
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Diagram 65-30. Start Read (Part 1) and End Operation

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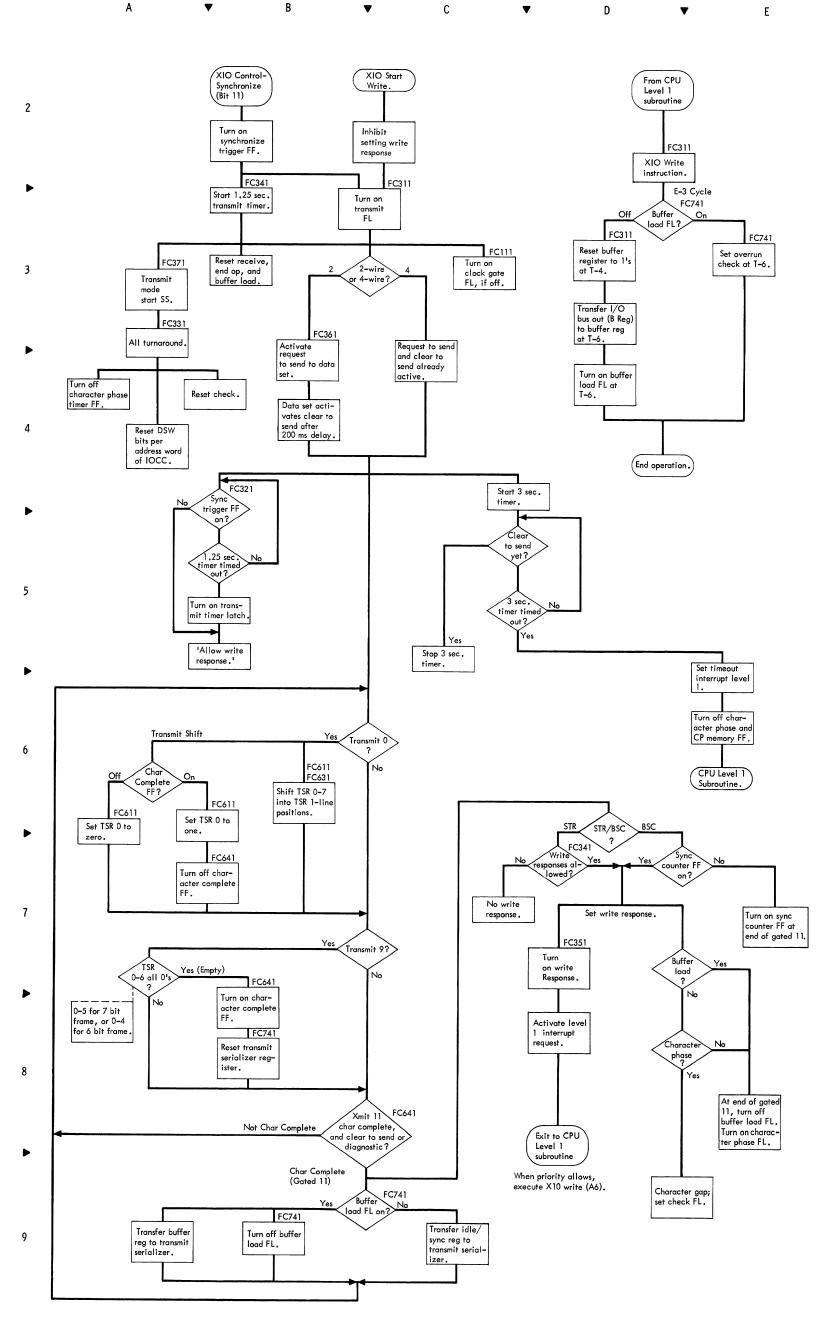
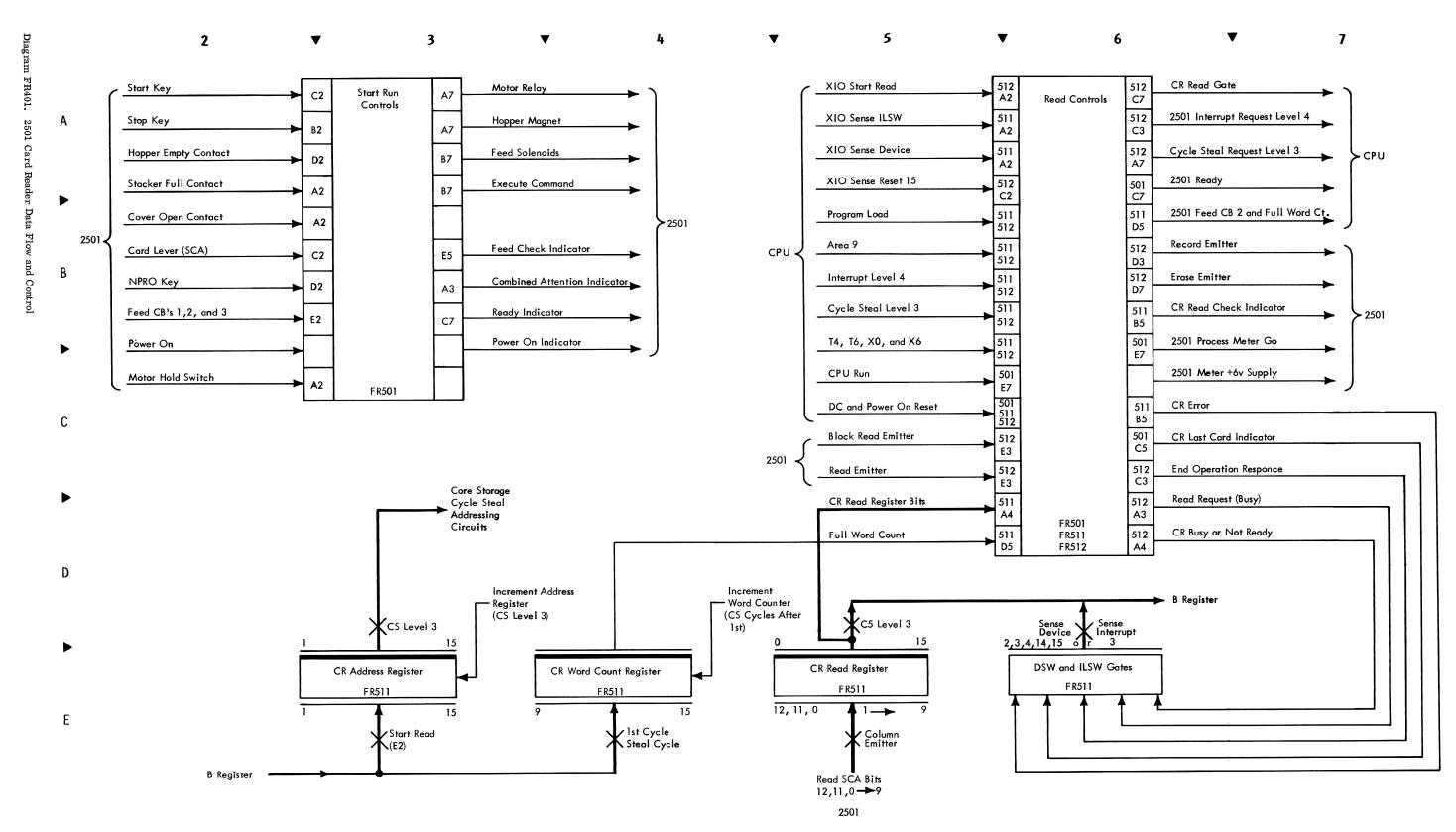


Diagram 65-50. Synchronize, Start Write, and Write



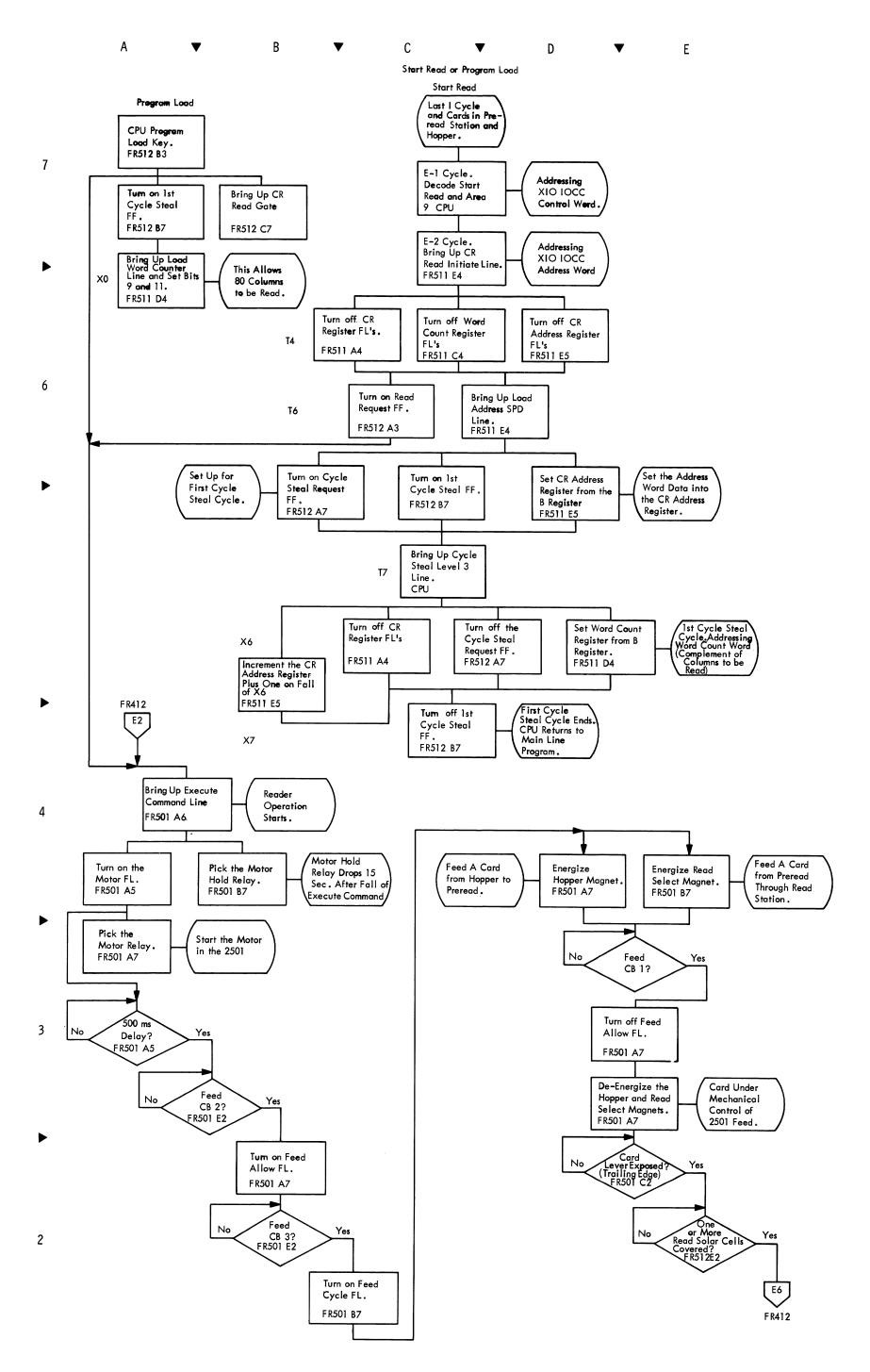


Diagram FR411. 2501 Start Read or Program Load (Part 1 of 2)

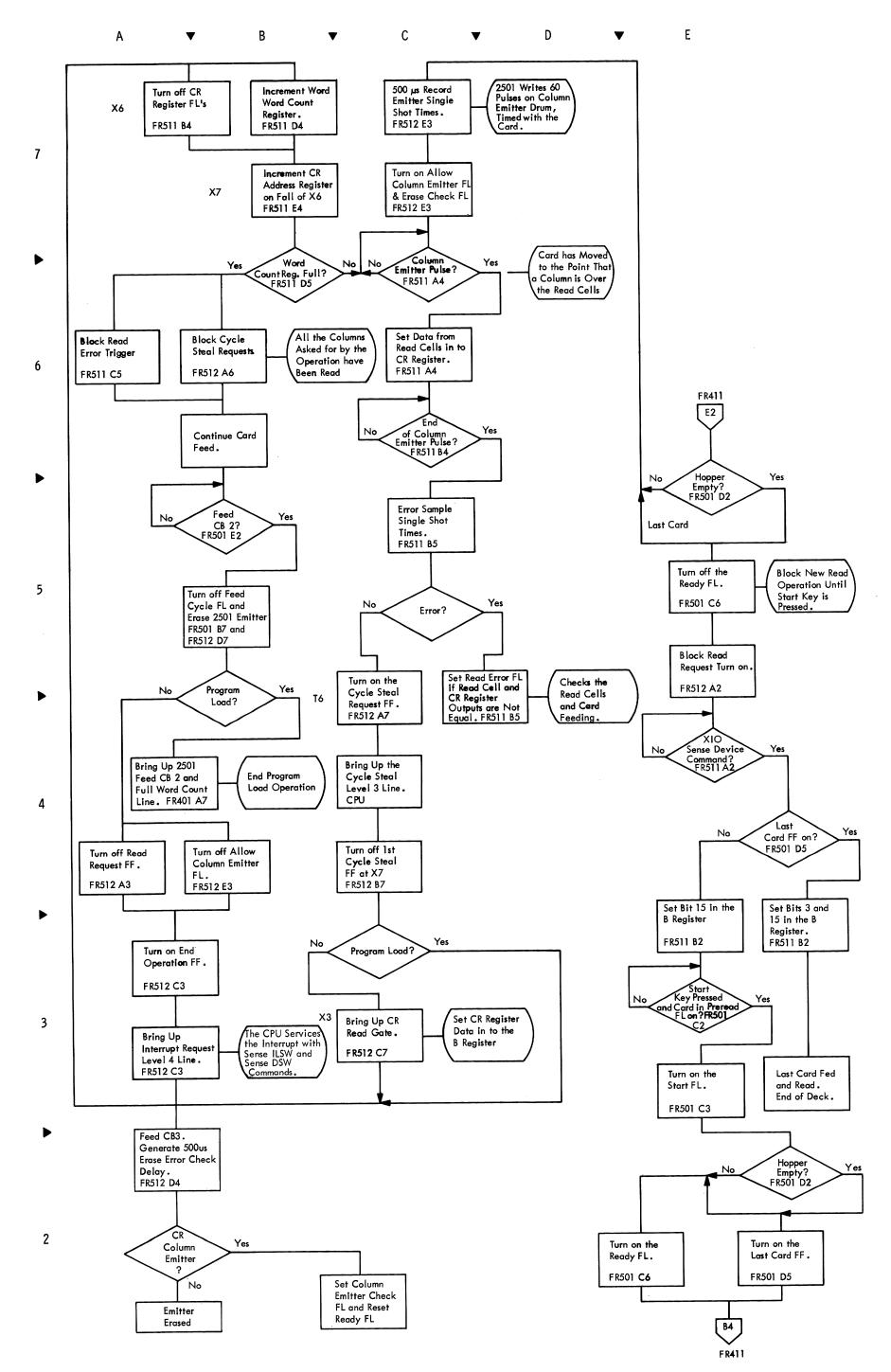


Diagram FR412. 2501 Start Read or Program Load (Part 2 of 2)

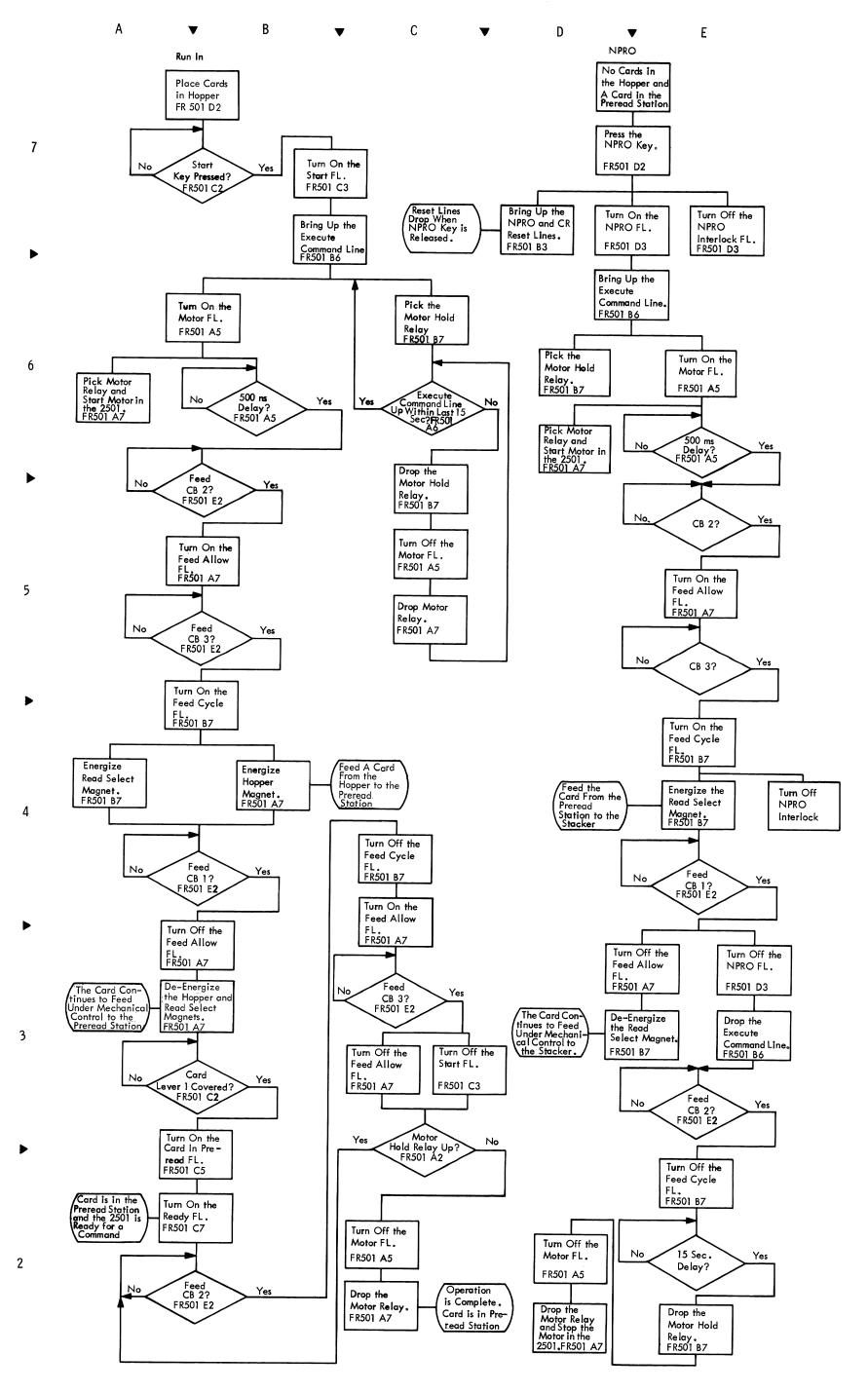
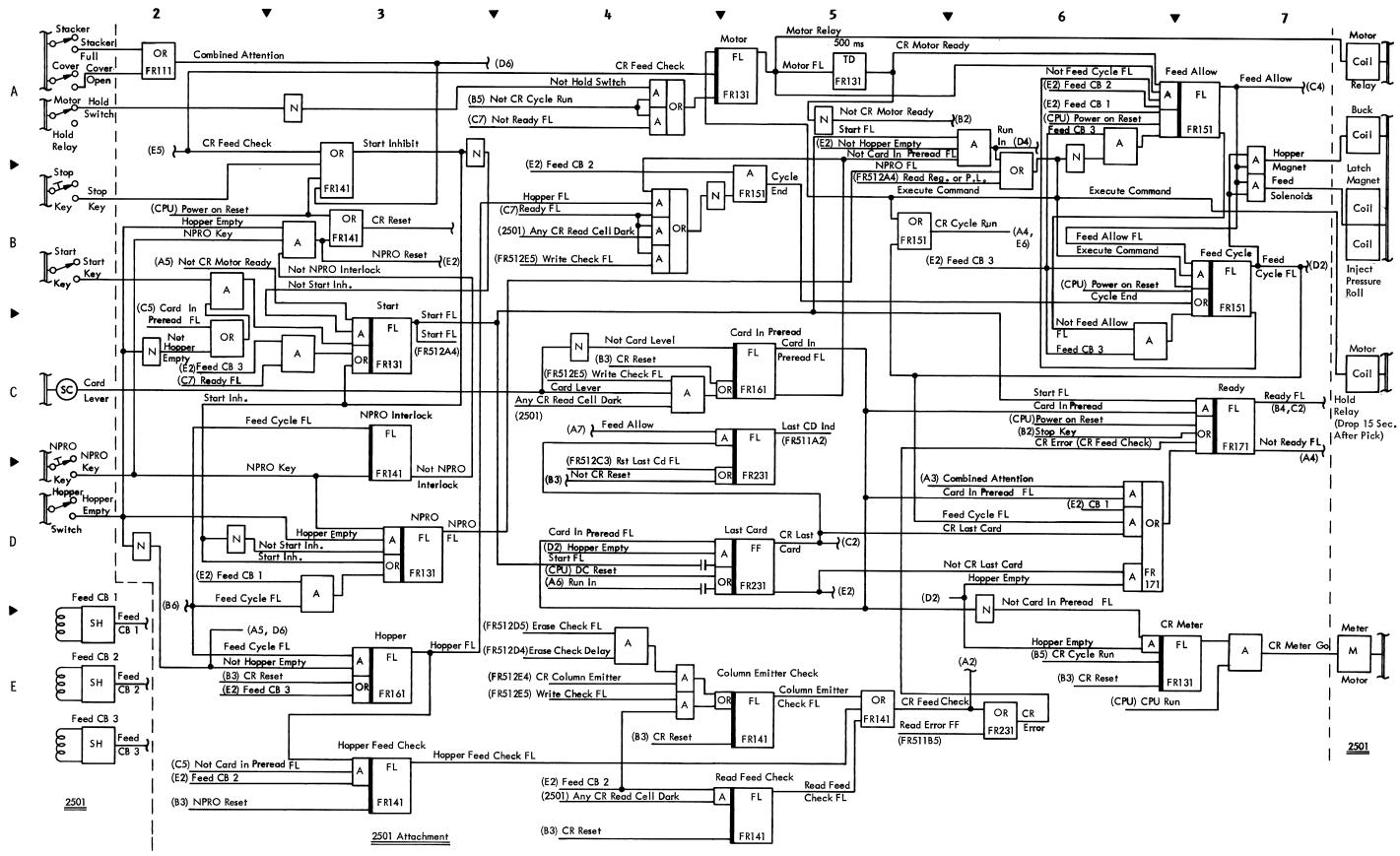
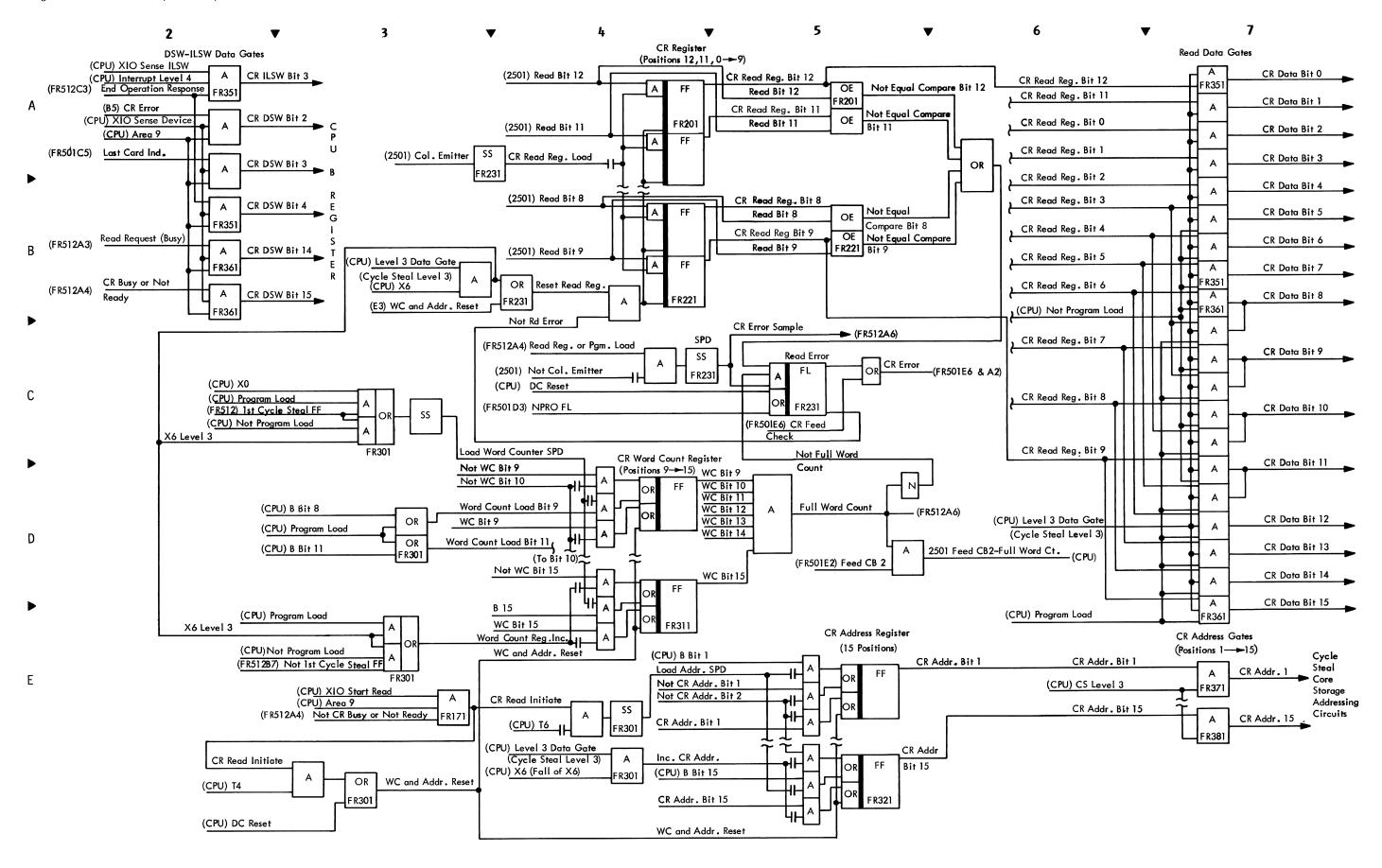
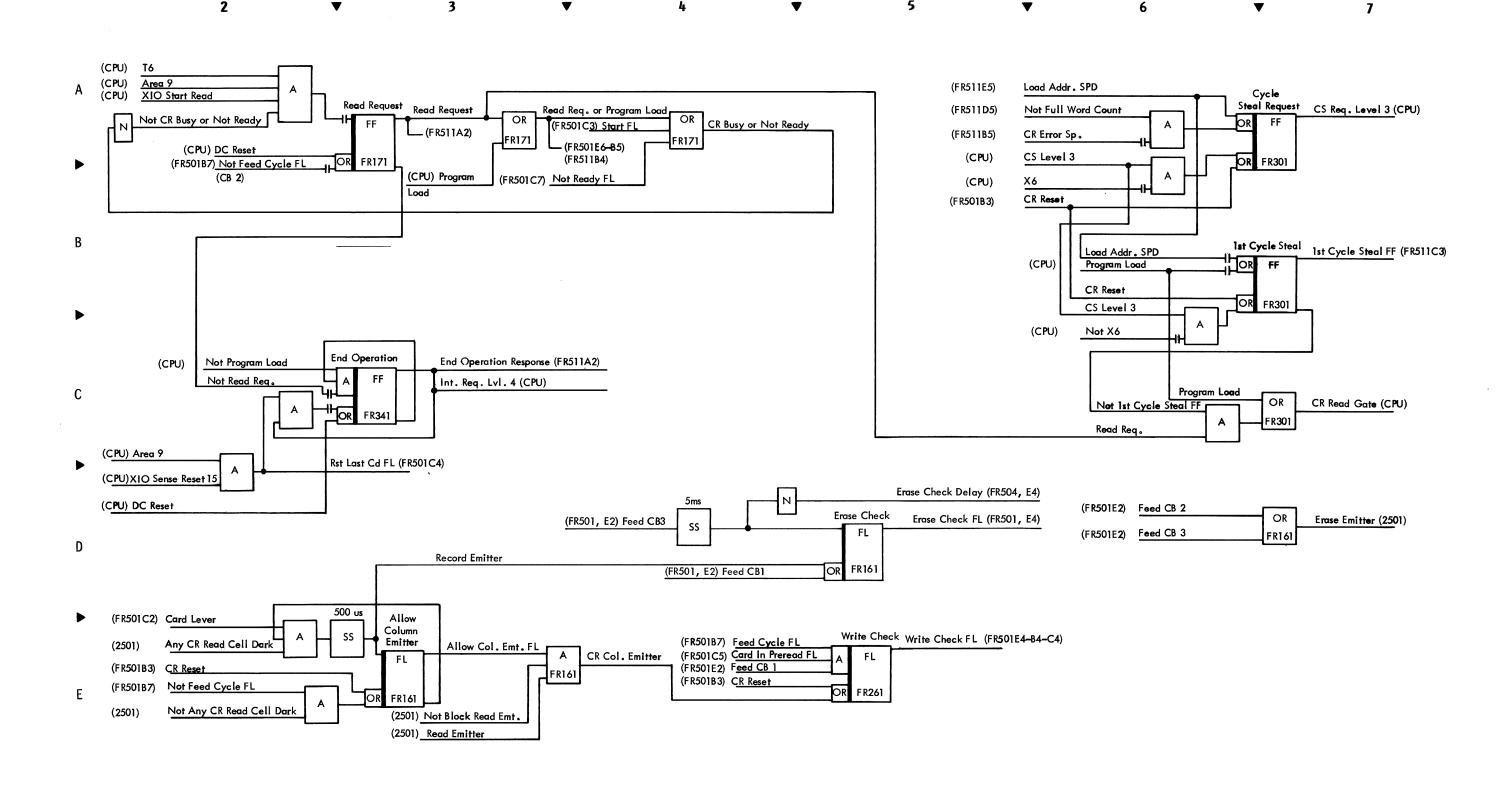


Diagram FR413. 2501 Run In - NPRO







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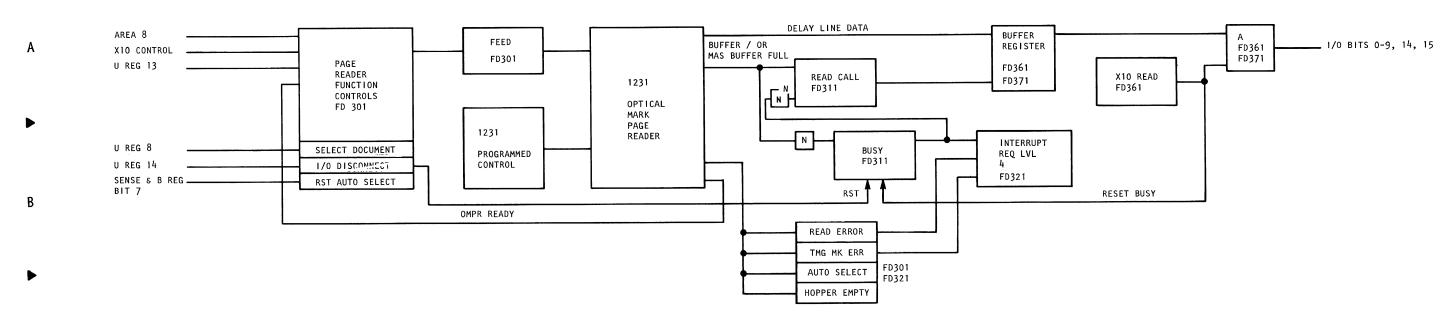
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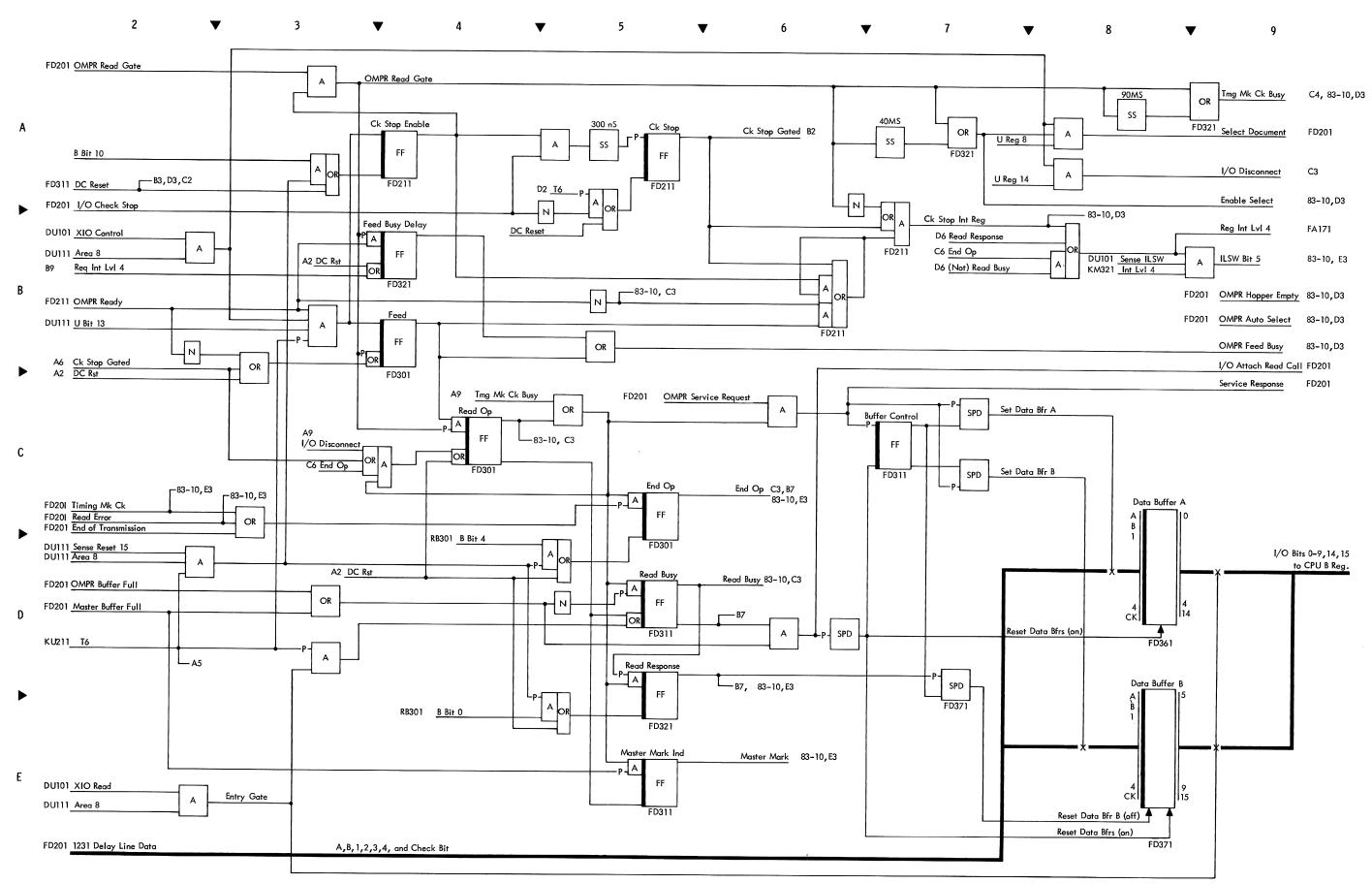


2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7



C	B5		15	OMPR IS NOT READY
	C4		14	OMPR READ OP
	D6		13	READ BUSY
<b>&gt;</b>		DSW		NEAD BOST
		AND ILSW	$\vdash$	
	В7	BITS FOR	10	CHECK STOP INT. REQ.
D	В9	1231	9	OMPR HOPPER IS EMPTY
	А9	FD301	8	OMPR TIMING MARK CHECK BUSY
	В9	FD311	7	I/O SELECTED DOCUMENT (Auto Select)
<b>•</b>	В9	FD321	6	OMPR FEED BUSY
	А9		5	OMPR OK TO SELECT DOCUMENT (Enable Select)
	С6		4	OMPR OPERATION COMPLETE (End Op)
	E6		3	MASTER MARK
E	C2		2	OMPR READ ERROR
	C 2		1	TIMING MARK CHECK
	D6		0	OMPR READ RESPONSE
	В9		П	1231 ILSW BIT 5

Note: References in left column are co-ordinates for Diagram 84-10.



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